THE JIM WILLIAMS PAPERS

High-speed communications circuits

High-frequency communications signals need wideband analog circuits. High-speed monolithic amplifiers let you build simple, effective circuits to meet this need for both optical and RF transmission.

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Megahertz-range data transmission and communications requires wideband linear circuitry. By designing around a monolithic high-speed amplifier, you can easily implement a variety of standard high-performance communications circuits. The following circuits detail several such designs for both optical and RF transmission. All have been carefully worked out and can serve as good idea sources.

Amplifying fast photodiode signals over a wide range of optical intensity is one common optical-communications requirement. **Fig 1a**'s fast FET amplifier gives wideband operation for 5 decades of photocurrent. You set up the photodiode in the conventional manner and *use a −15V bias to aid diode response.* Photocurrent feeds directly to IC_1's summing point, which causes IC_1's output signal to move to whatever level is required to maintain virtual ground at the negative input pin. **Fig 1b** details the circuit's operating characteristics when using the HP5082-4204 photodiode.

You must use care when frequency-compensating this circuit. The diode has approximately 2 pF of parasitic capacitance, which creates a significant lag at IC_1's summing point. Without a feedback capacitor, the circuit's high-speed dynamics are poor. **Fig 1c** illustrates this point by showing the circuit's response to a photocurrent input pulse (trace A) when the 3-pF feedback capacitor is removed. IC_1's output voltage (trace B) overshoots and saturates before finally ringing down to its final value. Replacing the feedback capacitor gives **Fig 1d**'s results. The same input pulse (trace A) produces a cleanly damped output voltage (trace B). The capacitor, however, imposes a 50% speed penalty (note that the horizontal scale of **Fig 1d** is faster than that of **Fig 1c**). This penalty is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

Basic amplifier has many uses

You can use the basic photodiode amplifier as the foundation for a variety of measurement and communications circuits. One such measurement circuit is **Fig 2a**'s photointegrator. The output voltage represents the integral of the diode's photocurrent over a time period defined by the control line. This circuit is par-

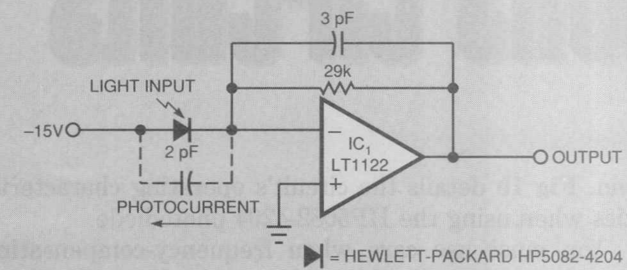
ticularly useful for measuring the total energy in a light pulse or pulses. The circuit is a fast integrator and uses IC_{2A} as a reset switch. IC_{2B}, which the control input signal switches simultaneously with IC_{2A}, compensates for IC_{2A}'s charge-injection error.

When the control input line is low (**Fig 2b,** trace A) and no photocurrent is present, IC_{2A} is closed and IC_1 acts as a grounded follower. Under these conditions, IC_1's output signal (trace C) sits at 0V. When the control input line goes high, IC_1 becomes an integrator as soon as IC_{2A} opens. Due to the switch delay, IC_2 opens approximately 150 nsec after the control input line goes high.

When IC_{2A} opens, it delivers some parasitic charge to IC_1's summing point. IC_{2B} provides a compensatory charge-based pulse at IC_1's positive terminal to cancel the effects of IC_{2A}'s charge error. The combined effect of the two charge pulses shows up as a fast, small amplitude event in IC_1's output, which settles rapidly back to 0V. You can see this event on trace C near the 400-nsec mark.

Once the switches have opened, the integrator is ready to receive and record a light pulse. When a light pulse (trace B) falls on the photodiode, IC_1 responds by integrating (trace C). With the circuit as shown in **Fig 2a,** IC_1 integrates rapidly until the light pulse ceases. IC_1's voltage after the light event is over is related to the total energy the photodiode sees during the event. In typical operation, the control line then returns low, which resets IC_1 for the next light event.

When the circuit has only 10 pF of integration capacitance, its output droop rate is about 0.2V/µsec. You

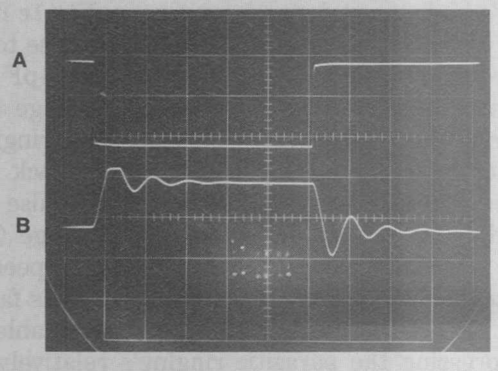


(a)

RESPONSE DATA

LIGHT (900 nm)	DIODE CURRENT	CIRCUIT OUTPUT
1 mW	350 µA	10.0V
100 µW	35 µA	1V
10 µW	3.5 µA	0.1V
1 µW	350 nA	0.01V
100 nW	35 nA	0.001V

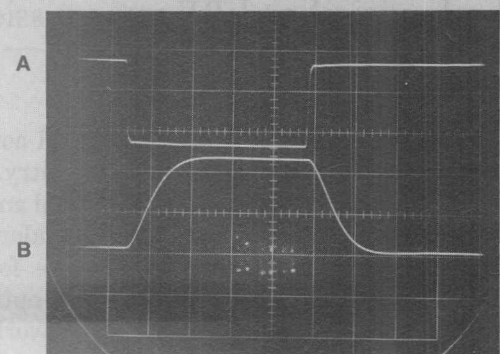
(b)



HORIZONTAL SCALE=500 nSEC/DIV

TRACE	VERTICAL SCALE
A	175 µA/DIV
B	10V/DIV

(c)



HORIZONTAL SCALE=200 nSEC/DIV

TRACE	VERTICAL SCALE
A	175 µA/DIV
B	5V/DIV

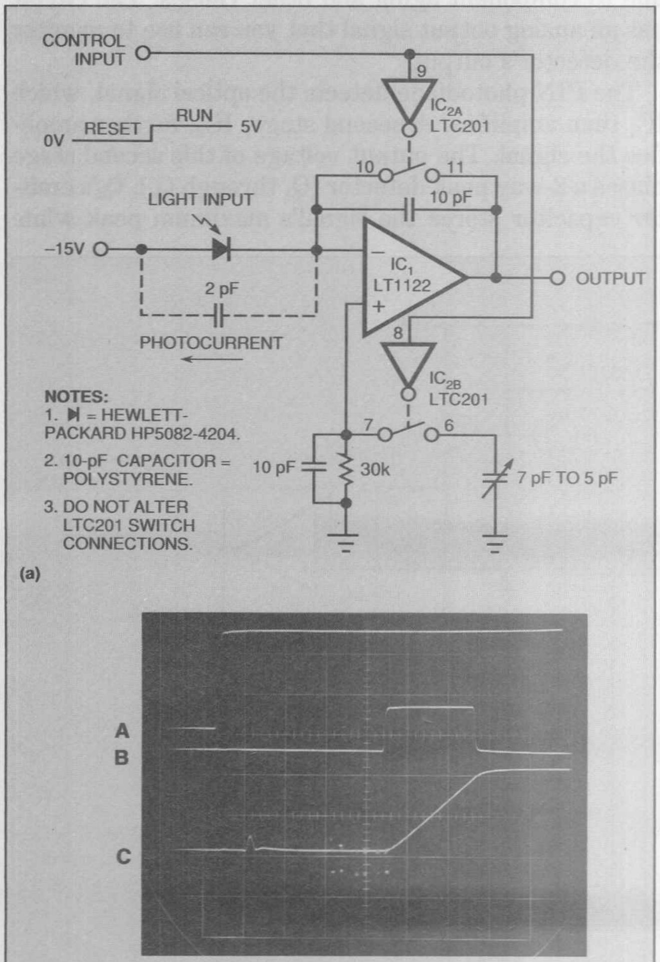
(d)

Fig 1—This basic photodiode amplifier circuit ***(a)*** *handles 5 decades of light intensity. The table* ***(b)*** *details the circuit's operating characteristics with the HP5082-4204 diode. Parts* ***c*** *and* ***d*** *show the circuit's response (trace B) to an input signal (trace A) without and with compensation, respectively.*

can increase the capacitance, but the integration speed will suffer accordingly. As shown, the circuit accommodates integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes. Thus, light pulses with optical-power intensities spanning microwatts to milliwatts over wide ranges of duration are practical input signals.

The primary factors restricting the circuit's accuracy are IC_1's 75-pA bias current and 12V output swing and the effectiveness of the charge-cancellation network. Typically, the circuit can achieve full-scale accuracy within several percent if you trim the charge-cancellation network. To trim the network, make sure that no light falls on the diode while you repetitively pulse the control line. Adjust the trimmer capacitor to achieve a 0V output at IC_1 immediately after the disturbance associated with the IC_{2A}-IC_{2B} switching settles.

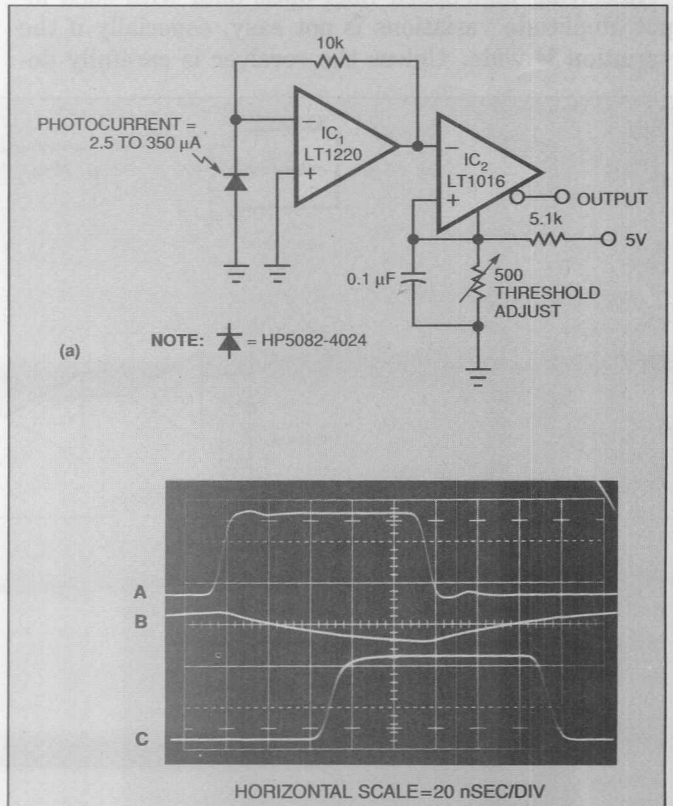
A communications circuit that relies on the basic photodiode amplifier is the simple fiber-optic receiver in **Fig 3a.** IC_1, a photocurrent-to-voltage converter similar to **Fig 1a,** feeds comparator IC_2. IC_2 compares IC_1's output voltage to a dc level established by the



TRACE	VERTICAL SCALE
A	2V/DIV
B,C	5V/DIV

(b)

*Fig 2—The basic photodiode amplifier is the basis for this integrator, which has a resettable output (**a**). When the control line is high (**b**, trace A), the circuit integrates (trace C) the incoming signal (trace B).*



TRACE	VERTICAL SCALE
A	5V/DIV
B	0.2V/DIV
C	2V/DIV

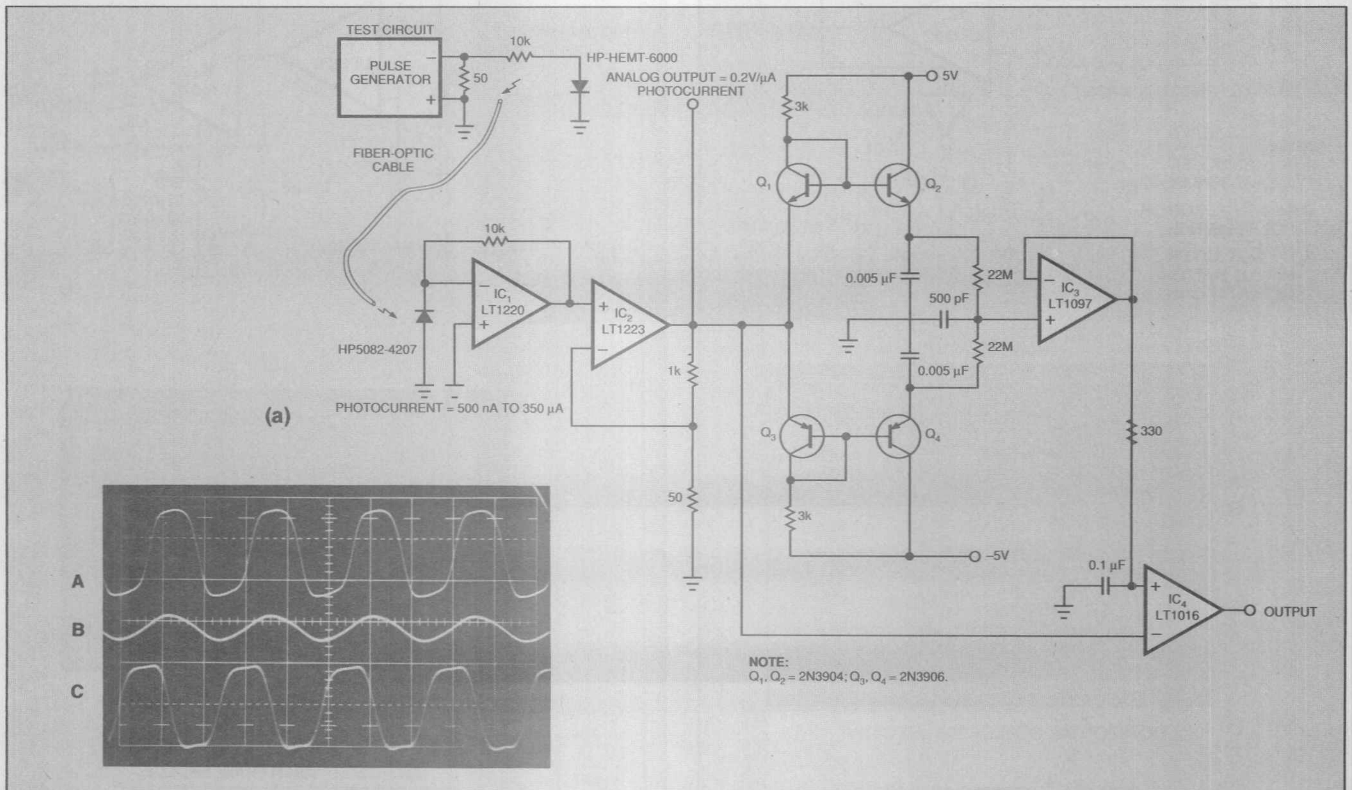
(b)

*Fig 3—This simple optical receiver (**a**) has a fixed signal threshold. The outputs of IC_1 (**b**, trace B) and IC_2 (trace C) lag the input signal (trace A).*

threshold-adjust potentiometer, thus producing a logic-compatible output signal. **Fig 3b** shows this circuit's typical waveforms. Trace A is a pulse associated with a light input signal. Trace B is IC_1's response, and trace C is IC_2's output signal. The phase shift between the photocurrent input signal and IC_2's output signal is due to IC_1's delay in reaching the threshold level. Reducing the threshold level will help reduce the shift but moves the circuit's operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and the fiber-optic line over time and temperature. These response changes manifest as changes in the apparent amplitude of the signal.

Receiving high-speed fiber-optic data with such input amplitude variations is not easy, especially if the variation is wide. Unless the receiver is carefully designed, the high-speed data and uncertain intensity of the light level can cause erroneous results. **Fig 4a** addresses the previous circuit's fixed-threshold limitation and offers significant performance advantages. This receiver reliably conditions fiber-optic input signals as fast as 40 MHz. The peak-to-peak amplitude of input signal can vary by as much as 40 dB. The circuit's digital output stage has an adaptive threshold trigger that accommodates signal intensity variations due to component aging and other causes. The circuit has an analog output signal that you can use to monitor the detector's output.

The PIN photodiode detects the optical signal, which IC_1 then amplifies. A second stage, IC_2, further amplifies the signal. The output voltage of this second stage biases a 2-way peak detector (Q_1 through Q_4). Q_2's emitter capacitor stores the signal's maximum peak while



HORIZONTAL SCALE=20 nSEC/DIV

TRACE	VERTICAL SCALE
A	5V/DIV
B,C	2V/DIV

(b)

***Fig 4—A self-adapting threshold** is the hallmark of this optical receiver (**a**). Driven by a test signal (**b**, trace A), the circuit lets you monitor the detector's current (trace B) in addition to producing a final output (trace C).*

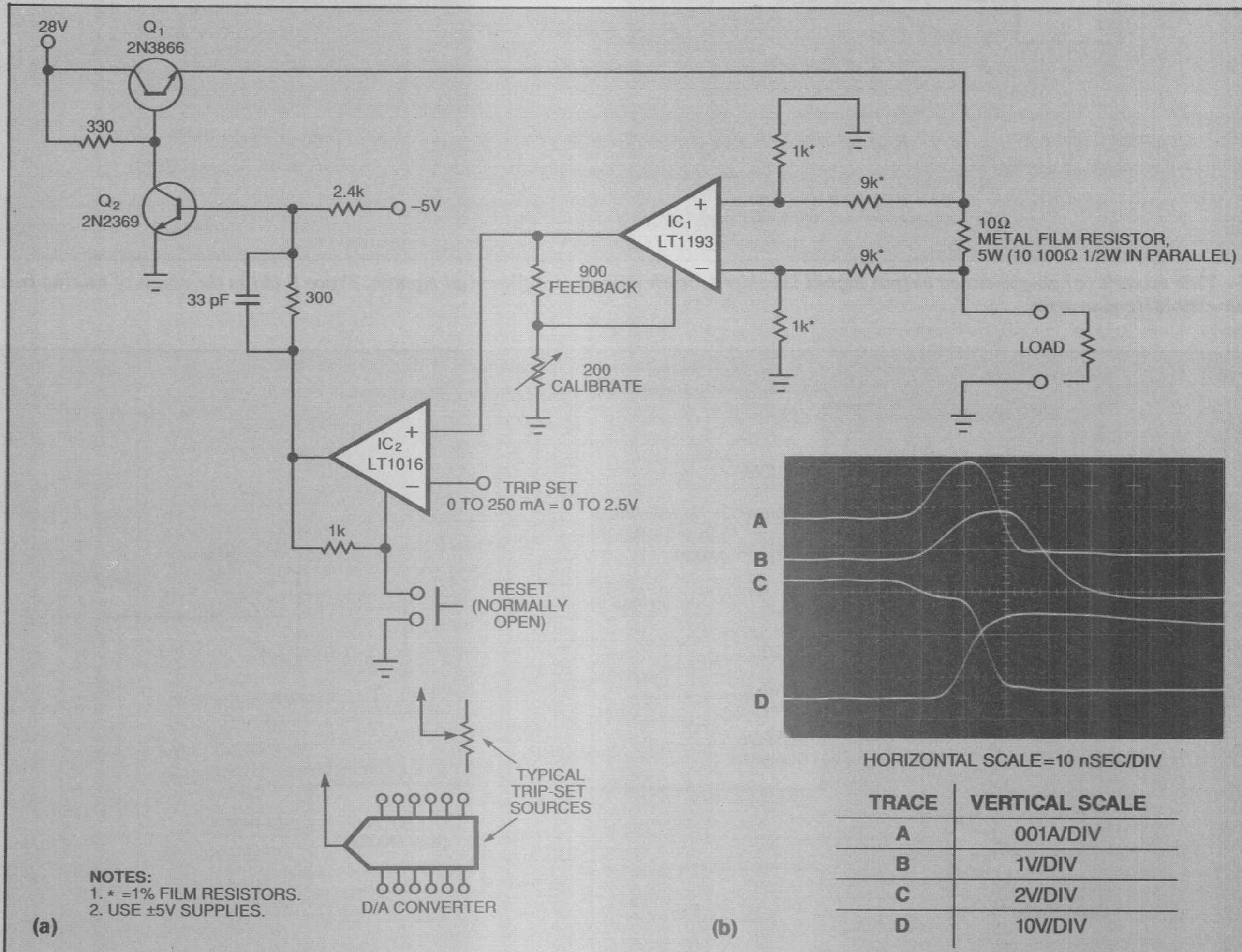
Protective circuit can save you a load

Some type of fuse or circuit breaker helps protect integrated circuits during developmental probing and expensive loads during trimming and calibration. **Fig Aa** shows a simple circuit that will turn off current in a load 18 nsec after that current exceeds a preset value. The circuit is especially versatile because one side of the load is grounded.

Under normal conditions, Q_1's emitter is biased on and supplying power to the load via the 10Ω current shunt. Differential amplifier IC_1's output signal resides below comparator IC_2's voltage-programmed trip point, and Q_2 is off.

When an overload occurs, Q_1's emitter current begins to increase (**Fig Ab**, trace A, just prior to the third vertical division). IC_1's output voltage (trace B) begins to rise as it tracks the increase in voltage across the 10Ω shunt. The 9-kΩ, 1-kΩ voltage dividers keep IC_1's input pins within their common-mode range. Q_1's emitter voltage (trace C) begins to drop as the transistor beta-limits. When IC_1's version of the load current exceeds IC_2's trip point, IC_2 goes high (trace D), which turns on Q_2. (Local positive feedback at IC_2's latch pin causes IC_2 to latch in this off state.) Q_2 steals Q_1's base drive, thus turning off the load current.

Once you've cleared the load fault, you can use the push button to reset the circuit. The delay from the onset of excessive load current to complete circuit shutdown is less than 18 nsec. (When interpreting the **Fig Ab** waveforms, note that trace A's current probe has a 4-nsec delay.) To calibrate the circuit, ground Q_2's base and install a 250-mA load. Adjust the 200Ω trim for a 2.5V output signal at IC_1. Next, remove the load, unground Q_2's base, and press the reset button. Finally, set the desired trip voltage, and the circuit is ready for use.



TRACE	VERTICAL SCALE
A	001A/DIV
B	1V/DIV
C	2V/DIV
D	10V/DIV

Fig A—This circuit breaker (a) trips in as little as 18 nsec. The circuit shuts down the load (b, trace C) when the load current (trace A) exceeds the trip point. Trace B represents IC_1's output voltage; trace D represents IC_2's output voltage.

Q_4's emitter capacitor retains the minimum excursion. The dc value of the midpoint of IC_2's output signal appears at the junction of the 500-pF capacitor and the 22-MΩ resistors. This point will always be midway between the signal's excursions, regardless of the signal's absolute amplitude. The low-bias LT1097 op amp (IC_3) buffers this signal-adaptive voltage to set the trigger voltage at IC_4's positive input pin. IC_4's negative input pin is biased directly from IC_2's output.

Fig 4b shows the results of using the test circuit of **Fig 4a**. The pulse generator's output signal is trace A; IC_2's analog output voltage is trace B. IC_4's output signal is trace C. The waveforms were recorded using a 5-μA photocurrent at about 20 MHz as the test signal.

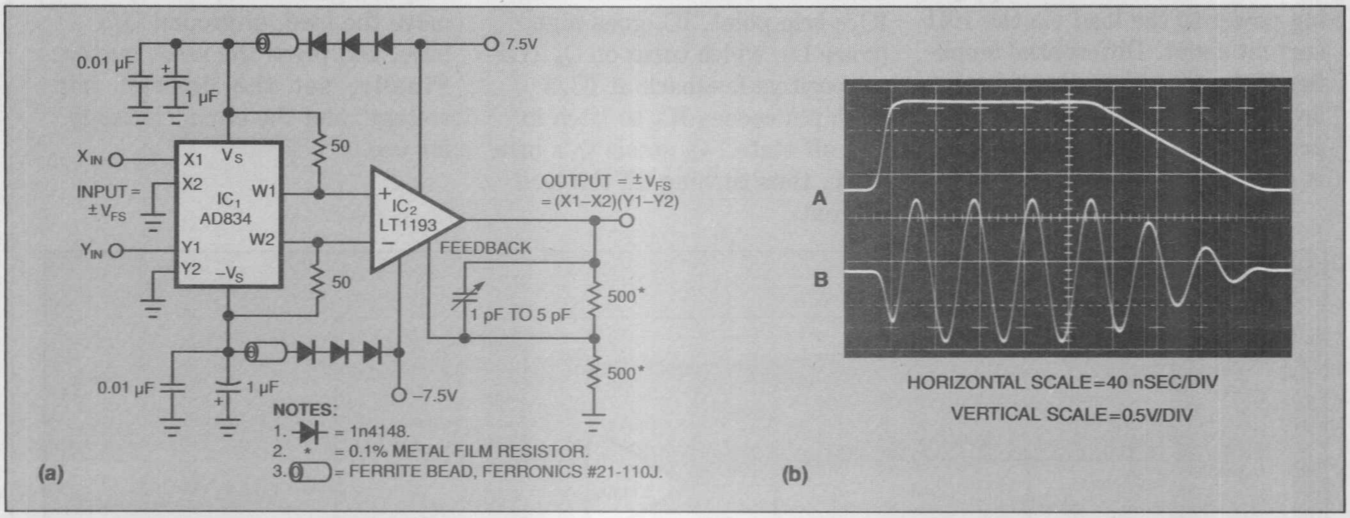


Fig 5—This mixer's ***(a) single-ended output signal*** *is easier to work with than differential signals. Trace B* ***(b)*** *is the result of mixing trace A with a 20-MHz sine wave.*

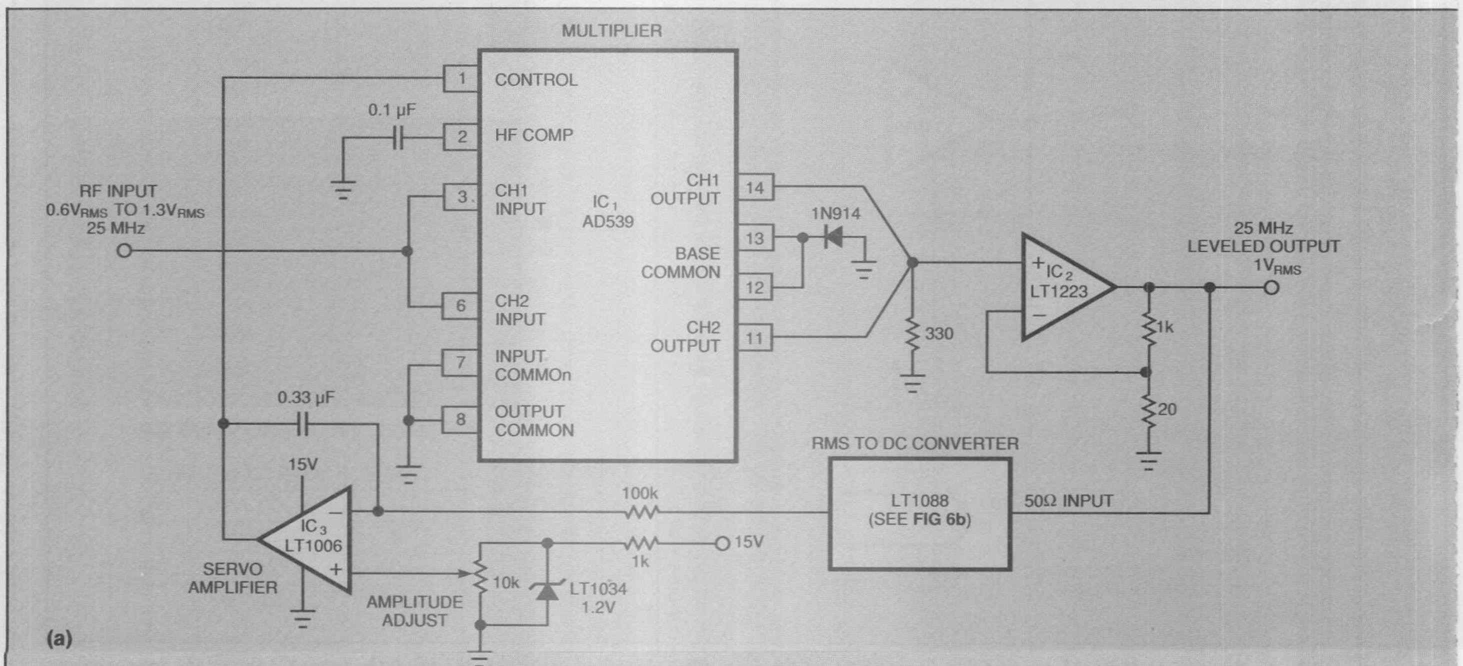


Fig 6—A servo loop enables this circuit to stabilize *RF signals. The loop circuit* ***(a)*** *uses an rms-to-dc converter* ***(b)***.

Note that IC_4's output transitions (trace C) correspond with the midpoint (plus IC_4's 10-nsec propagation delay) of IC_2's output signal (trace B), in accordance with the adaptive-trigger circuit's operation.

Mixer yields single-ended signal

Another common communications requirement, particularly for RF work, is mixing signals for modulation or heterodyning. Analog multipliers can mix signals, but they have a drawback; their output signals take a differential form. These differential signals, which have substantial common-mode content, are frequently inconvenient to work with. You can use RF transformers to convert them to single-ended signals, but you lose dc and low-frequency information in the process. **Fig 5a** illustrates a better approach. The circuit uses the LT1193 differential amplifier (IC_2) to accomplish the differential-to-single-ended transition. Set up IC_1 in the configuration **Ref 1** recommends. The LT1193 takes the differential signal from IC_1's 50Ω-terminated output lines and provides a single-ended output signal. The amplifier's gain of 2 yields an 11V output signal at full scale.

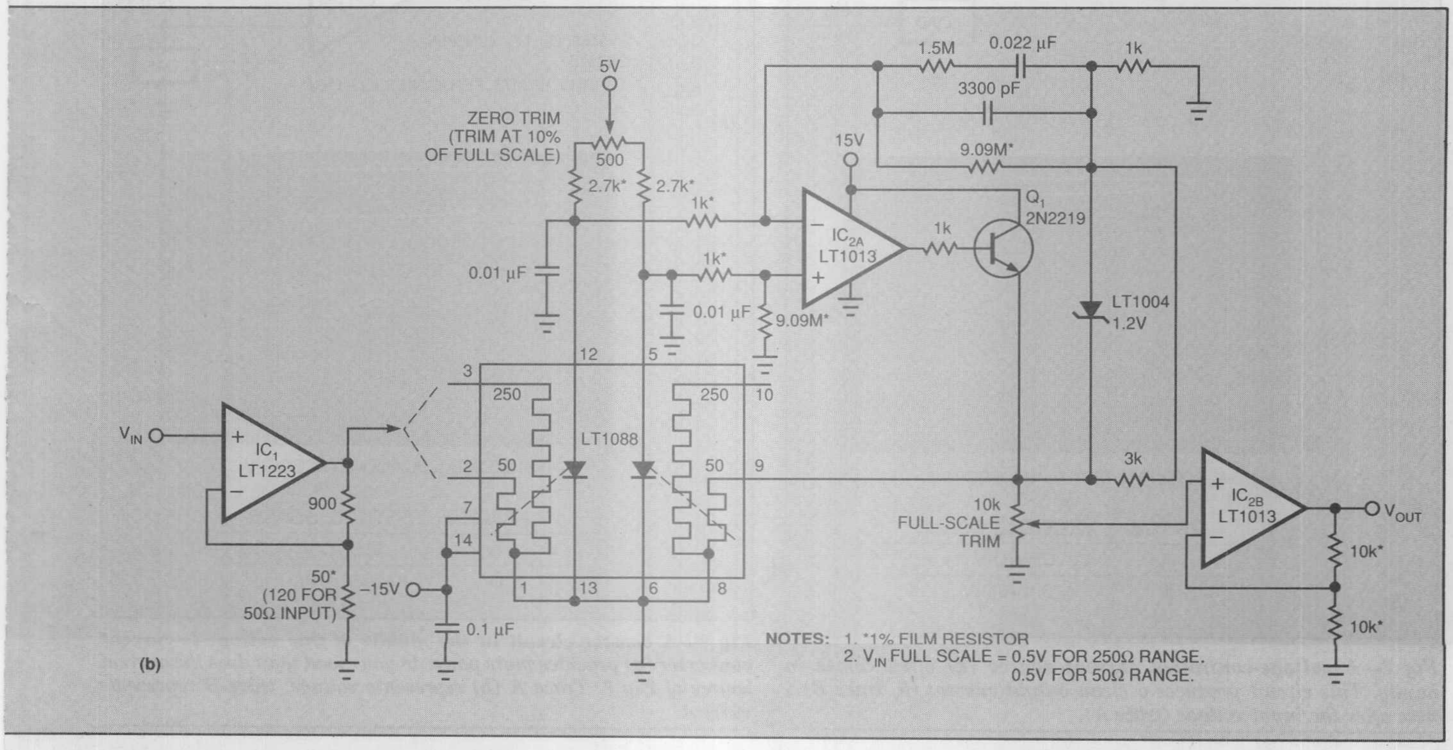
IC_1's output signals ride on a common-mode level quite close to the device's positive supply. This common-mode level falls outside IC_2's input common-mode range. The diodes in the 7.5V supply rails drop the supply voltage to IC_1, which biases IC_1's output signals within IC_2's input range. This scheme avoids the attenuation and matching problems you'd get if you placed a level shift between the multiplier and amplifier. The impedance of the ferrite beads combine with the diodes' impedance to ensure adequate bypassing for the multiplier.

Acronyms used in this article

FET—Field-effect transistor
RF—Radio frequency
rms—Root mean square

This circuit's performance is quite impressive. Error remains within 2% over dc to 50 MHz, and feedthrough is less than −50 dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square-wave peaking. **Fig 5b** shows the circuit's performance when multiplying a 20-MHz sine wave by trace A's waveform. The output signal (trace B) is a singularly clean instantaneous representation of the X and Y input products.

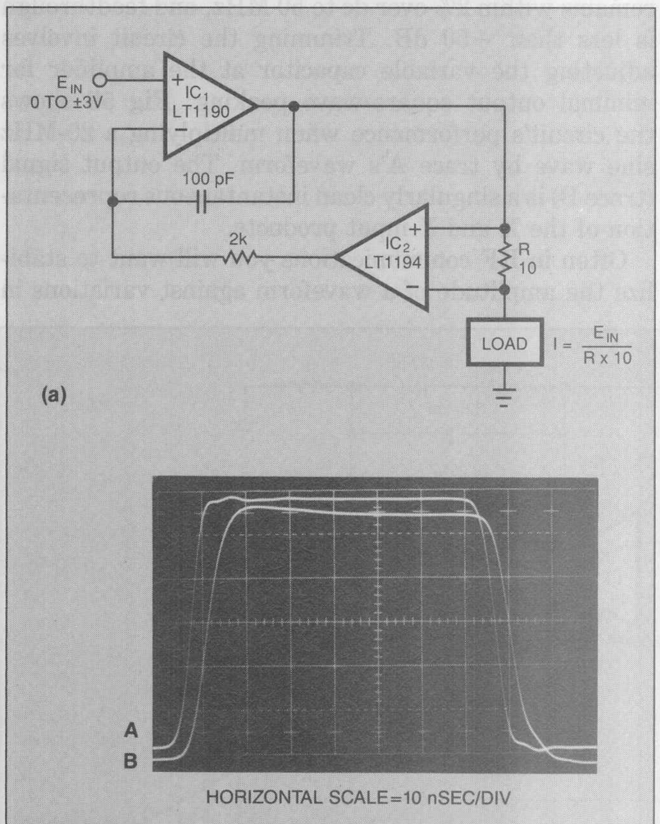
Often in RF communications you will want to stabilize the amplitude of a waveform against variations in



input signal strength over time and temperature. Instruments and transmitters must often provide this function, which is not easy if the instruments must also maintain waveform purity. **Fig 6a** shows a circuit that stabilizes waveform amplitudes while maintaining waveform purity.

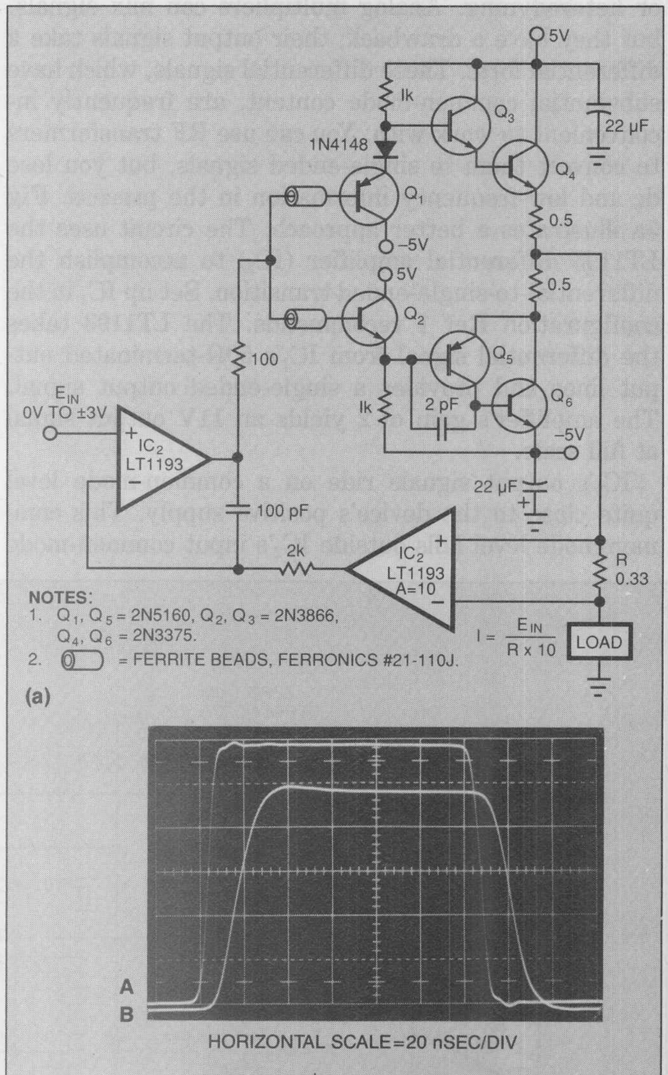
You apply the RF input signal to the AD539 wideband multiplier (IC_1), which drives IC_2. An LT1088-based rms-to-dc converter **(Fig 6b)** turns IC_2's output to dc. A servo amplifier (IC_3) compares that dc output signal with a settable dc reference and biases the multiplier's control channel, thus completing a loop. The 0.33-μF capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo amplifier. The loop maintains the output's 25-MHz rms amplitude at the dc reference's value; it rejects changes in load, input-signal strength, power-supply voltage, and other variables.

All of the previous circuits have a voltage-based output signal. Sometimes, however, you'll want your output in current form. **Fig 7a** shows a voltage-controlled current source that has both the load and control voltage referenced to ground. This simple, powerful circuit produces output current in accordance with the sign



TRACE	VERTICAL SCALE
A	0.5V/DIV
B	5 mA/DIV

*Fig 7—A voltage-controlled current source **(a)** often comes in handy. This circuit produces a clean output current (**b**, trace B) 4 nsec after the input voltage (trace A).*



TRACE	VERTICAL SCALE
A	0.5V/DIV
B	0.2A/DIV

*Fig 8—A booster circuit in the middle of this voltage-to-current converter **(a)** provides more power to your load than does the current source of **Fig 7**. Trace A **(b)** represents voltage; trace B represents current.*

and magnitude of the control voltage. Resistor R sets the circuit's scale factor.

IC_1, biased by E_{IN}, drives current through R (in this case 10Ω) and the load. IC_2, sensing the differential voltage across R, closes a loop back to IC_1. The load current is constant because IC_1's loop forces a fixed voltage across R. The 2-kΩ, 100-pF combination sets roll-off, and the configuration is stable. **Fig 7b** shows the circuit's dynamic response. Trace A is the control input voltage, E_{IN}; trace B is the output current. The response has a delay of 5 nsec and no slew residue or aberrations.

Fig 8a is **Fig 7a**'s basic current source plus a 1A booster stage to increase output power. Including the booster inside IC_1's feedback loop eliminates the booster's dc errors. Note that the booster needs no current-limiting features because of the circuit's inherent current-limiting operation. **Fig 8b** shows that the circuit's response is as clean as that of the lower-power version, although its delay is about 20 nsec slower. The loop stability considerations involved in placing IC_2 and the booster in IC_1's feedback path are significant. This type of circuit receives detailed treatment in **Ref 2**. EDN

References

1. Analog Devices Inc, *Linear Products Databook*, AD834 Datasheet, pgs 6-43.
2. Williams, Jim, "Subduing high-speed op-amp problems," *EDN*, October 24, 1991, pg 135.

Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.

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